Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended): A method for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said method comprising:

configuring said I/O pin to be used to transmit and receive pulses [[data]];

indicating ~~generating~~ logical ones using first pulses that are a first width ~~length~~ and indicating ~~generating~~ logical zeros using second pulses that are a second width ~~length~~; and

communicating with said device by transmitting and receiving said first and second pulses via said I/O pin. ~~utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.~~

2. (Original): The method according to claim 1, further comprising the steps of:

configuring said I/O pin by connecting said I/O pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and

said I/O pin being configured as an open collector output that will serve as both an input pin and an output pin.

3. (Currently amended): The method according to claim 1, further comprising the steps of:

generating said first and second pulses ~~logical ones and logical zeros~~ using an external device that is coupled to said device using said I/O pin.

4. (Original): The method according to claim 3, further comprising the steps of:

connecting a first node of a second resistor included within said external device to a power source;

connecting a second node of said second resistor to a first node of an LED;

connecting a second node of said LED to a first communication pin of said external device;

connecting said second node of said LED to a first node of a switch; and

connecting a second node of said switch to ground.

5. (Currently amended): The method according to claim 4, further comprising the steps of:

connecting said first communication pin of said external device to said I/O pin of said device; and

generating said first and second pulses ~~logical ones and logical zeros~~ by opening and closing said switch.

6. (Currently amended): The method according to claim 5, further comprising the steps of:

generating a bit stream by repeatedly opening and closing said switch to generate said first and second pulses ~~logical ones and said logical zeros~~;

generating said first pulses ~~logical ones~~ by closing said switch for a first length of time; and

generating said second pulses ~~logical zeros~~ by closing said switch for a second length of time.

7. (Currently amended): The method according to claim 5, further comprising the steps of:

connecting said first communication pin of said external device to said I/O pin of said device; and

receiving, by said first communication pin of said external device, said first and second pulses [[data]] transmitted by device utilizing said I/O communication pin; and

outputting said first and second pulses [[data]] using said LED.

8. (Original): The method according to claim 3, further comprising the steps of:

connecting a first node of a bi-directional driver that is included in said external device to a first communication pin of said external device; and

connecting said first communication pin to said I/O pin of said device.

9. (Currently amended): The method according to claim 8, further comprising:

generating said first and second pulses ~~logical ones and said logical zeros~~ by said external device and outputting said first and second pulses ~~logical ones and said logical zeros~~ using said first communication pin.

10. (Currently amended): A system for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said system comprising:

said I/O pin being configured to both transmit and receive pulses [[data]];

logical ones being indicated using first pulses that are a first width and logical zeros being indicated using second pulses that are a second width; and

~~said I/O pin for receiving and transmitting logical ones that are pulses that are a first length and logical zeros that are pulses that are a second length; and~~

said I/O pin for transmitting and receiving said first and second pulses to communicate with said device. ~~communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.~~

11. (Original): The system according to claim 10, further comprising:

said I/O pin being configured by connecting said I/O pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and

said I/O pin being configured as an open collector output that will serve as both an input pin and an output pin.

12. (Currently amended): The system according to claim 10, further comprising:

said first and second pulses ~~logical ones and logical zeros~~ being generated using an external device that is coupled to said device using said I/O pin.

13. (Original): The system according to claim 12, further comprising:

a first node of a second resistor included within said external device connected to a power source;

a second node of said second resistor connected to a first node of an LED;

a second node of said LED connected to a first communication pin of said external device;

said second node of said LED connected to a first node of a switch; and

a second node of said switch connected to ground.

14. (Currently amended): The system according to claim 13, further comprising:

said first communication pin of said external device connected to said I/O pin of said device; and

said first and second pulses ~~logical ones and logical zeros~~ being generated by opening and closing said switch.

15. (Currently amended): The system according to claim 14, further comprising:

a bit stream generated by repeatedly opening and closing said switch to generate said first and second pulses ~~logical ones and said logical zeros~~;

said first pulses ~~logical ones~~ generated by closing said switch for a first length of time; and

said second pulses ~~logical zeros~~ generated by closing said switch for a second length of time.

16. (Currently amended): The system according to claim 14, further comprising:

said first communication pin of said external device connected to said I/O pin of said device; and

said first communication pin of said external device for receiving said first and second pulses [[data]] transmitted by device utilizing said I/O communication pin; and

said LED for outputting said first and second pulses [[data]].

17. (Original): The system according to claim 12, further comprising:

a first node of a bi-directional driver that is included in said external device connected to a first communication pin of said external device; and

said first communication pin connected to said I/O pin of said device.

18. (Currently amended): The system according to claim 17, further:

said first and second pulses ~~logical ones and said logical zeros~~ generated by said external device and outputting said first and second pulses ~~logical ones and said logical zeros~~ using said first communication pin.

19. (Currently amended): A computer program product for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said product comprising:

instructions for configuring said I/O pin to be used to transmit and receive pulses [[data]];

instructions for indicating ~~generating~~ logical ones using first pulses that are a first width ~~length~~ and indicating ~~generating~~ logical zeros using second pulses that are a second width ~~length~~; and

instructions for communicating with said device by transmitting and receiving said first and second pulses via said I/O pin, ~~utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.~~

20. (Currently amended): The product according to claim 19, further comprising:

instructions for generating a bit stream by repeatedly opening and closing a switch that is external to said device and connected to said I/O pin to generate said first and second pulses ~~logical ones and said logical zeros~~;

instructions for generating said first pulses ~~logical ones~~ by closing said switch for a first length of time; and

instructions for generating said second pulses ~~logical zeros~~ by closing said switch for a second length of time.